BIRAD
RESEARCH & DEVELOPMENT

CUTTING-EDGE COMPLEMENTARY **DUAL MODULAR REDUNDANCY MEMORY CELL**

The Problem

Embedded memories are often operated at scaled supply voltages in order to reduce their power consumption. However, reduction in the supply voltage also increases their susceptibility to soft errors. Soft errors occur when an energetic particle hits a reversed bias junction of an internal node in a memory cell, possibly flipping the data stored in it. Embedded memory errors are typically handled at an architectural level with error-correction-codes or triple-modular redundancy, incurring high area overhead, delay and complexity.

The Solution

Our proposed novel, complementary dual modular redundancy (CDMR) memory is based on a four transistor dynamic memory core that internally stores complementary data values to provide an inherent per-bit error detection capability.

The Commercial Benefit

By adding simple, low-overhead parity, our memory:

- Has an added error-correction capability
- Displays as much as a 3.5x smaller silicon footprint than other radiation-hardened bitcells (when implemented in a 65nm CMOS technology)
- Saves between 48%– 87% standby power than other considered solutions across the entire operating region

Market Potential

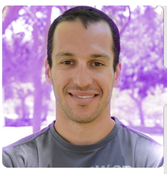
The non-volatile memory market is expected to be worth USD 82.03 Billion by 2022, at a CAGR of 9.50% between 2017 and 2022. The growth of this memory market is driven by customers' need for high-speed, low-power-consuming, and highly scalable memory devices.

Target Markets/Industries

- Automotive
- Artificial intelligence
- Low-power
- Wireless communications
- Smart-cards

Intellectual Property

Patent pending



Team: Primary Inventor

Mr. Robert Giterman

Robert Giterman is currently pursuing the Ph.D. degree under Prof. Alex Fish as part of the Emerging Nanoscaled Intergrated Circuits and Systems (EnICS) Lab in Bar Ilan University. Mr. Giterman's research interests include embedded DRAM design and optimization for low power and high performance operation, SRAM design with an emphasis on improved stability, error-correction and fault-tolerant circuits and development of hardware-security oriented embedded memories for use in low-power applications and high-end processors. As part of his research, Robert Giterman led several full test chip integrations and tape out. Giterman has authored/ and co-authored over 15 journal articles and international conference papers and 5 patent applications, and has presented his research at a number of international conferences.
In 2014, Robert Giterman was awarded the presidential scholarship for outstanding Doctorate students. In 2016, he was awarded with the Lev-Zion Scholarship for excellent Ph.D. Students. In 2017 Robert Giterman was awarded with the Katz Scholarship.

Future Research

Migration and adjustment to below 10nm technologies

The Opportunity

Investors are invited to license our patent through a licensing agreement with sponsored research.

Keywords

- Single event upset
- Soft errors
- Embedded DRAM
- Gain cell
- Radiation hardening
- SRAM
- Space applications