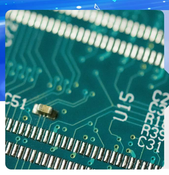
BIRAD
RESEARCH & DEVELOPMENT



GAIN CELL EMBEDDED DRAM IN FULLY DEPLETED SILICON-ON-INSULATOR TECHNOLOGY

The Problem

As technology dimensions continue to scale down, high density embedded memories are of great interest for many VLSI systems. However, 6T SRAM cells incur a large area penalty and suffer from high static power consumption in scaled CMOS nodes, often dominating the total area and power budget of a system. Gain-Cell embedded DRAM (GC-eDRAM) is an alternative to SRAM, featuring high density, non-destructive readout, low leakage, and two-port operation. However, GC-eDRAM:

- Requires refresh cycles to maintain data, with the refresh operation becoming the main power consumer in deeply scaled technology nodes.
- Suffers from high access latency compared to SRAM due to degraded levels in the cell. Hence, large design guard bands and performance margins are needed to ensure reliable operation under process variability.

The Solution

Anti-Microbial & Anti-biofilm

We propose a novel GC-eDRAM implementation in FD-SOI technology, which significantly improves the data retention time and access latency using body biasing.

The Commercial Benefit

Our cutting-edge, unique innovative structure:

- Enables the usage of body-bias to extend the cell's DRT using reversed body bias
- Improves the read access latency using forward body bias.
- Provides per-bit error detection capabilities with low area overhead
- Offers 50% reduction in area over SRAM
- Allows 30% DRT improvement over conventional GC-eDRAM without body bias.

Market Potential

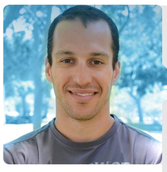
In 2017, global embedded systems market was valued at around USD 86 billion. This market is expected to reach USD 114 billion in 2024, growing at a CAGR of 4.0% between 2018 and 2024.

Target Markets/Industries

- Automotive
- Artificial intelligence
- Low-power
- Wireless communications
- Smart-cards

Intellectual Property

Patent pending



Team: Primary Inventor

Mr. Robert Giterman

Robert Giterman is currently pursuing the Ph.D. degree under Prof. Alex Fish as part of the Emerging Nanoscaled Intergrated Circuits and Systems (EnICS) Lab in Bar Ilan University. Mr. Giterman's research interests include embedded DRAM design and optimization for low power and high performance operation, SRAM design with an emphasis on improved stability, error-correction and fault-tolerant circuits and development of hardware-security oriented embedded memories for use in low-power applications and high-end processors. As part of his research, Robert Giterman led several full test chip integrations and tape out. Giterman has authored/ and co-authored over 15 journal articles and international conference papers and 5 patent applications, and has presented his research at a number of international conferences.
In 2014, Robert Giterman was awarded the presidential scholarship for outstanding Doctorate students. In 2016, he was awarded with the Lev-Zion Scholarship for excellent Ph.D. Students. In 2017 Robert Giterman was awarded with the Katz Scholarship.

Future Research

Development and optimization of advanced features in 28nm silicon.

The Opportunity

We invite investors to license our patent through a licensing agreement with a sponsored research.

Keywords

- GC-eDRAM
- embedded memories
- low power
- body biasing