BIRAD
RESEARCH & DEVELOPMENT

Novel High Density **Memory Macro**

The Problem

Due to the growing demand for high-density embedded memories in modern microprocessors and other VLSI Systemon- Chip (SoC) designs, gain cell embedded DRAM (GCeDRAM) has emerged as an alternative to static random access memory (SRAM). GCeDRAM is known for its high-density, non-destructive read operation, low leakage power, and two-port operation. However, GCeDRAM requires periodic refresh cycles to reliable retain data, both reducing the memory availability and consuming dynamic refresh power. While GC-eDRAM Implementations in mature technology nodes, such as 90 nm and 65 nm, provides long data retention time (DRTs), sub nm technologies suffer from much shorter DRTs due to the reduced parasitic storage capacitances and increased leakage currents.

The Solution

We propose a novel memory macro suitable for deeply scaled CMOS technologies and high-bandwidth applications.

The Commercial Benefit

Our innovative memory macro:

- Is fully logic compatible
- Provides dual-ported functionality
- Can be operated at above 500Mhz
- Provides over 30% lower area and power compared to an SRAM memory in the same technology
- Contains high-speed differential sense amplifier and low-threshold readout transistors for improved access time
- Contains level converting write drivers for improved write in terms of both speed and level passing

The proposed technology was fabricated in a 28nm CMOS bulk process, demonstrating up-to 800 MHz operating frequency, over 10us of data retention time, and a 30% area reduction over conventional SRAM memories.

Market Potential

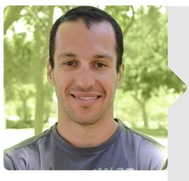
The non-volatile memory market is expected to be worth USD 82.03 Billion by 2022, at a CAGR of 9.50% between 2017 and 2022. The growth of this memory market is driven by customers' need for high-speed, low-power-consuming, and highly scalable memory devices.

Target Markets/Industries

- Automotive
- Artificial intelligence
- Low-power
- Wireless communications
- Smart-cards

Intellectual Property

Patent pending



Team: Primary Inventor

Mr. Robert Giterman

Robert Giterman is currently pursuing the Ph.D. degree under Prof. Alex Fish as part of the Emerging Nanoscaled Intergrated Circuits and Systems (EnICS) Lab in Bar Ilan University.

Mr. Giterman's research interests include embedded DRAM design and optimization for low power and high performance operation, SRAM design with an emphasis on improved stability, error-correction and fault-tolerant circuits and development of hardware-security oriented embedded memories for use in low-power applications and high-end processors. As part of his research, Robert Giterman led several full test chip integrations and tape out.

Giterman has authored/ and co-authored over 15 journal articles and international conference papers and 5 patent applications, and has presented his research at a number of international conferences..

In 2014, Robert Giterman was awarded the presidential scholarship for outstanding Doctorate students. In 2016, he was awarded with the Lev-Zion Scholarship for excellent Ph.D. Students. In 2017 Robert Giterman was awarded with the Katz Scholarship.

Future Research

ImplemenQtation and verification in FQinFET technology

The Opportunity

Companies are welcome to license our patent through a licensing agreement or through sponsored research.

Keywords

- Gain cell
- Logic-compatible eDRAM
- SRAM
- Low power
- High density
- High bandwidth